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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2181	5

DATE MAILED: 11/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/866,005	SCHMISSEUR ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 23 May 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 24 and 25 recite the limitation "The processing system of Claim 17" in Line 1 of Claim 24. There is insufficient antecedent basis for this limitation in the claim as Claim 17 is directed to an article.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4, 5, 7, 8, 9, 10, 12, 13, 15, 16, 21, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,734,847 to Garbus et al. ("Garbus") and Revision 2.2 of the PCI Local Bus Specification.

A secondary reference can be used in a rejection under 35 USC §102 in order to show an inherent characteristic of the thing taught by the primary reference.

> "To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that

the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991)" (See MPEP §2131.01).

In reference to Claim 1, Garbus teaches a peripheral device (See Figure 1 Numbers 9, 11, and 13) accessible through a data interface (See Figure 1 Number 5 and Figure 2 Numbers 29, 33, and 35) with a data bus (See Figures 1 and 2 Number 15). Garbus does not expressly state that the peripheral devices define a plurality of device functions. However, Garbus does state that the devices are intended to represent any device that conforms with the PCI Local Bus Specification (See Column 4 Lines 42-43). The PCI Local Bus Specification teaches that a device can contain up to eight separate functions and that individual functions of a device can be addressed (See Section 3.2.2.3.1, Page 31). Therefore, the devices of Garbus are inherently adapted to define a plurality of device functions that can be individually addressed. Garbus further teaches that the I/O processor can support and control private PCI devices (analogous to a first processing system adapted to communicate with a first device function of the peripheral device through the data interface) (See Column 8 Lines 27-28); and that commands received by the primary interface of the bridge are converted to configure devices connected to the secondary interface of the bridge (analogous to the second processing system adapted to communicate with a second function of the peripheral device through the data interface) (See Column 5 Lines 4-6 and 36-39).

In reference to Claim 4, Garbus teaches the limitations as applied to Claim 1 above. Garbus further teaches the second processing system (See Figure 1 Number 3)

coupled to the data bus (See Figures 1 and 2 Number 15) through a bridge (See Figure 2 Number 29); and the first processing system being a peripheral device (See Figure 1 Number 5 and Figure 2 Number 21).

In reference to Claim 5, Garbus teaches the limitations as applied to Claim 1 above. Garbus further teaches that the first processing system comprises logic to cause a peripheral device to conceal one or more device functions from the second processing system (See Column 8 Lines 20-25).

In reference to Claim 7, Garbus teaches the limitations as applied to Claim 5 above. Garbus further teaches a bridge (See Figure 1 Number 5) coupled to the peripheral devices through a secondary bus (See Figure 1 Number 15) and wherein the bridge comprises logic to initiate execution of an enumeration process by the first processing system prior to completion of an enumeration process by the second processing system (See Figure 6 and Column 11 Lines 35-57).

In reference to Claim 8, Garbus teaches the limitations as applied to Claim 5 above. Garbus further teaches that the first processing system asserts a signal to a peripheral device in order to make it a private device (analogous to inhibiting enumeration of the peripheral device by the second processing system) (See Figure 3b and Column 7 Lines 46-63).

In reference to Claim 9, Garbus teaches a first enumeration procedure at a first processing system to enumerate a first device coupled to a data interface of a data bus (See Figure 1 and Figure 6 Number 211); and a second enumeration procedure at a second processing system to enumerate a second device (See Figure 1 and Figure 6

Number 215). Garbus does not expressly state that the peripheral devices define a plurality of device functions. However, Garbus does state that the devices are intended to represent any device that conforms with the PCI Local Bus Specification (See Column 4 Lines 42-43). The PCI Local Bus Specification teaches that a device can contain up to eight separate functions and that individual functions of a device can be addressed (See Section 3.2.2.3.1, Page 31). Therefore, the devices of Garbus are inherently adapted to define a plurality of device functions that can be individually addressed.

In reference to Claim 10, Garbus teaches the limitations as applied to Claim 9 above. Because all devices on the bus of Garbus are I/O devices (analogous to an I/O channel) (See Column 2 Lines 66-67 and Column 3 Lines 1-4), it is inherent that the enumerated device functions are associated with an I/O channel.

In reference to Claim 12, Garbus teaches the limitations as applied to Claim 9 above. Garbus further teaches the second processing system (See Figure 1 Number 3) coupled to the data bus (See Figures 1 and 2 Number 15) through a bridge (See Figure 2 Number 29); and the first processing system being a peripheral device (See Figure 1 Number 5 and Figure 2 Number 21).

In reference to Claim 13, Garbus teaches the limitations as applied to Claim 9 above. Garbus further teaches that the first processing system comprises logic to cause a peripheral device to conceal one or more device functions from the second processing system (See Column 8 Lines 20-25).

In reference to Claim 15, Garbus teaches the limitations as applied to Claim 13 above. Garbus further teaches a bridge (See Figure 1 Number 5) coupled to the peripheral devices through a secondary bus (See Figure 1 Number 15) and wherein the bridge comprises logic to initiate execution of an enumeration process by the first processing system prior to completion of an enumeration process by the second processing system (See Figure 6 and Column 11 Lines 35-57).

In reference to Claim 16, Garbus teaches the limitations as applied to Claim 13 above. Garbus further teaches that the first processing system asserts a signal to a peripheral device in order to make it a private device (analogous to inhibiting enumeration of the peripheral device by the second processing system) (See Figure 3b and Column 7 Lines 46-63).

In reference to Claim 21, Garbus teaches a first enumeration procedure at a first processing system to enumerate a first device coupled to a data interface of a data bus (See Figure 1 and Figure 6 Number 211); and the first processing system asserting a signal to a peripheral device in order to make it a private device (analogous to inhibiting enumeration of the peripheral device by the second processing system) (See Figure 3b and Column 7 Lines 46-63). Garbus does not expressly state that the peripheral devices define a plurality of device functions. However, Garbus does state that the devices are intended to represent any device that conforms with the PCI Local Bus Specification (See Column 4 Lines 42-43). The PCI Local Bus Specification teaches that a device can contain up to eight separate functions and that individual functions of a device can be addressed (See Section 3.2.2.3.1, Page 31). Therefore, the devices of

Garbus are inherently adapted to define a plurality of device functions that can be individually addressed.

In reference to Claim 22, Garbus teaches the limitations as applied to Claim 21 above. Because all devices on the bus of Garbus are I/O devices (analogous to an I/O channel) (See Column 2 Lines 66-67 and Column 3 Lines 1-4), it is inherent that the first device function is enumerated as an I/O channel.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Garbus as applied to Claim 1 above, and further in view of US Patent Number 6,230,216 to Chambers et al. ("Chambers").

In reference to Claim 2, Garbus teaches the limitations as applied to Claim 1 above. Garbus further teaches that all devices on the bus are I/O devices (analogous to an I/O channel) (See Column 2 Lines 66-67 and Column 3 Lines 1-4), so it is inherent that all of the enumerated device functions are associated with an I/O channel. Garbus does not teach the first processing system comprising logic to enumerate each device

function associated with an I/O channel. Chambers teaches a processor that configures devices on a bus based on the configuration requirements those devices have (analogous to enumerating device functions associated with an I/O channel) (See Column 6 Lines 24-40).

One of ordinary skill in the art at the time the invention was made would combine the device of Garbus with the device of Chambers, resulting in the invention of Claim 2, in order to be in accordance with the PCI specification (See Column 6 Lines 24-25 of Chambers).

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Garbus and Chambers as applied to Claim 2 above, and further in view of US Patent Number 6,044,207 to Pecone et al. ("Pecone").

In reference to Claim 3, Garbus and Chambers teach the limitations as applied to Claim 2 above. Garbus and Chambers do not teach the device function associated with the I/O channel comprising logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

One of ordinary skill in the art at the time the invention was made would combine the device of Garbus and Chambers with the device of Pecone, resulting in the invention of Claim 3, in order to provide a method and apparatus for managing multiple independent disks in a manner that achieves a desired level of availability, efficiency,

capacity, performance, and economic cost of storing large quantities of readily available data in a data storage system (See Column 4 Lines 16-24).

7. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garbus as applied to Claims 5 and 13 above, and further in view of US Patent Number 6,094,699 to Surugucchi et al. ("Surugucchi").

In reference to Claim 6, Garbus teaches the limitations as applied to Claim 5 above. Garbus further teaches the first processing system enumerating a first device coupled to a data interface of a data bus (See Figure 1 and Figure 6 Number 211). Garbus does not teach logic to set information in a configuration header maintained at the peripheral device to conceal the first function from the second processing system. Surugucchi teaches a second processing system using select address signal lines to access the configuration register spaces (analogous to the configuration header) of the interface controllers (analogous to the peripheral devices) to conceal the controller from the second processing system (See Column 5 Lines 66-67 and Column 6 Lines 1-12).

In reference to Claim 14, Garbus teaches the limitations as applied to Claim 13 above. Garbus further teaches the first processing system enumerating a first device coupled to a data interface of a data bus (See Figure 1 and Figure 6 Number 211). Garbus does not teach setting information in a configuration header maintained at the peripheral device to conceal the first function from the second processing system. Surugucchi teaches a second processing system using select address signal lines to access the configuration register spaces (analogous to the configuration header) of the

interface controllers (analogous to the peripheral devices) to conceal the controller from the second processing system (See Column 5 Lines 66-67 and Column 6 Lines 1-12).

One of ordinary skill in the art at the time the invention was made would combine the device of Garbus with the device of Surugucchi, resulting in the inventions of Claims 6 and 14, in order to hide the devices from both the host system and the secondary bus (See Column 6 Lines 6-9 of Surugucchi).

8. Claims 11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garbus as applied to Claims 10 and 22 above, and further in view of Pecone.

In reference to Claim 11, Garbus teaches the limitations as applied to Claim 10 above. Garbus does not teach the device function associated with the I/O channel comprising logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

In reference to Claim 23, Garbus teaches the limitations as applied to Claim 22 above. Garbus does not teach the device function associated with the I/O channel comprising logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

One of ordinary skill in the art at the time the invention was made would combine the device of Garbus with the device of Pecone, resulting in the invention of Claims 11 and 23, in order to provide a method and apparatus for managing multiple independent

disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available data in a data storage system (See Column 4 Lines 16-24).

9. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garbus and US Patent Number 5,737,344 to Belser et al. ("Belser").

In reference to Claim 17, Garbus teaches a first enumeration procedure at a first processing system to enumerate a first device coupled to a data interface of a data bus (See Figure 1 and Figure 6 Number 211). Garbus further teaches that the PCI devices (See Figure 3b Numbers 47, 49, 51, 53, and 55) are connected to a bus, which is in turn connected to the Secondary PCI Interface (See Figure 3b Number 35), across which a signal is asserted to a peripheral device in order to make it a private device (analogous to initiating a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures) (See Figure 3b and Column 7

pressly state that the peripheral devices define a
ever, Garbus does state that the devices are intended
rms with the PCI Local Bus Specification (See
Local Bus Specification teaches that a device can
ons and that individual functions of a device can be
, Page 31). Therefore, the devices of Garbus are
rality of device functions that can be individually
ch that the method is stored as machine-readable

instructions on a storage medium. Belser teaches a processor that executes machine-readable instructions stored on a direct access storage device (See Column 4 Lines 5-15).

In reference to Claim 18, Garbus and Belser teach the limitations as applied to Claim 17 above. Because all devices on the bus of Garbus are I/O devices (analogous to an I/O channel) (See Column 2 Lines 66-67 and Column 3 Lines 1-4), it is inherent that the first device function is enumerated as an I/O channel.

One of ordinary skill in the art would combine the device of Garbus with the device of Belser, resulting in the inventions of Claims 17 and 18, in order to provide an increased robustness against losing the instructions necessary to operate the device of Garbus (See Column 2 Lines 43-45 of Belser).

10. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Garbus and Belser as applied to Claim 18 above, and further in view of Pecone.

In reference to Claim 19, Garbus and Belser teach the limitations as applied to Claim 18 above. Garbus and Belser do not teach the device function associated with the I/O channel comprising logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

One of ordinary skill in the art at the time the invention was made would combine the device of Garbus and Belser with the device of Pecone, resulting in the invention of Claim 19, in order to provide a method and apparatus for managing multiple

independent disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available data in a data storage system (See Column 4 Lines 16-24).

11. Claims 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garbus and Belser as applied to Claim 17 above, and further in view of Surugucchi.

In reference to Claim 20, Garbus and Belser teach the limitations as applied to Claim 17 above. Garbus and Belser do not teach initiating a bus transaction to set information in a configuration header maintained at the peripheral device to conceal the first device function from subsequent enumeration procedures. Surugucchi teaches a second processing system using select address signal lines to access the configuration register spaces (analogous to the configuration header) of the interface controllers (analogous to the peripheral devices) to conceal the controller from the second processing system (See Column 5 Lines 66-67 and Column 6 Lines 1-12).

In reference to Claim 24, Garbus and Belser teach the limitations as applied to Claim 17 above. Garbus and Belser do not teach initiating a bus transaction to set information in a configuration header maintained at the peripheral device to conceal the first device function from subsequent enumeration procedures. Surugucchi teaches a second processing system using select address signal lines to access the configuration register spaces (analogous to the configuration header) of the interface controllers

(analogous to the peripheral devices) to conceal the controller from the second processing system (See Column 5 Lines 66-67 and Column 6 Lines 1-12).

One of ordinary skill in the art at the time the invention was made would combine the device of Garbus and Belser with the device of Surugucchi, resulting in the inventions of Claims 20 and 24, in order to hide the devices from both the host system and the secondary bus (See Column 6 Lines 6-9 of Surugucchi).

12. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Garbus, Belser, and Surugucchi as applied to Claim 24 above, and further in view of US Patent Number 5,960,213 to Wilson ("Wilson").

In reference to Claim 25, Garbus, Belser, and Surugucchi teach the limitations as applied to Claim 24 above. Garbus further teaches that the data bus is a PCI data bus (See Figures 1 and 2 Number 15). Garbus, Belser, and Surugucchi do not teach the processing system initiating a bus transaction to modify data in a Header Type register of the configuration register. Wilson teaches a Delta unit (analogous to the processing system) sending signals to set a bit in the Header Type register of other devices (See Column 6 Lines 21-28).

One of ordinary skill in the art at the time the invention was made would combine the device of Garbus, Belser, and Surugucchi with the device of Wilson, resulting in the invention of Claim 25, in order to allow the host system to view the secondary PCI devices as a single multifunction device (See Column 6 Lines 7-10 of Wilson).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (8-5:30), Alt. Fridays (8-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-5631.

tjc

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